REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicant believes that Claims 1-28 are in condition for allowance, and allowance of the application is therefore requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231, on October 9, 2002.

Pat Slaback
Name

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Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

21. (New) A system, comprising:

an external memory circuit having one or more configuration data output terminals; and

a programmable logic device (PLD), the PLD comprising:

a programmable logic portion having a first vertical pitch and a first horizontal pitch;

an internal configuration memory having one or more configuration data input terminals coupled to the configuration data output terminals of the external memory circuit, and further having output terminals coupled to the programmable logic portion of the PLD;

an embedded core having a second vertical pitch and a second horizontal pitch, wherein the first vertical pitch and the second vertical pitch are different; and

a first interconnect layer coupled between the programmable logic portion of the PLD and the embedded core, the first interconnect layer having a set of pitches selected from:

(i) the first vertical pitch and the second horizontal pitch; and

(ii) the first horizontal pitch and the second vertical pitch.

22. (New) The system of Claim 21, wherein the external memory circuit comprises one of a group of integrated circuits comprising: an EEPROM, an EPROM, and a PROM.

23. (New) The system of Claim 21, wherein the programmable logic portion of the PLD is a field programmable gate array (FPGA).

24. (New) The system of Claim 21, wherein the embedded core is a microprocessor.

25. (New) The system of Claim 21, wherein the interconnect layer was routed using a routing program having as an input the set of pitches.

26. (New) The system of Claim 25, wherein the PLD comprises a second interconnect layer coupled between the programmable logic portion of the PLD and the embedded core.

27. (New) The system of Claim 26, wherein the set of pitches is divided for input to the routing program, wherein one pitch in the set of pitches is used for the first interconnect layer and the other pitch in the set of pitches is used for the second interconnect layer.

28. (New) The system of Claim 21, wherein the first horizontal pitch and the second horizontal pitch are also different.